Digital System Design (CBCGS) Mock Paper for September 2020

Q		M
1.	The characteristic equation of an S-R flip-flop is a. Qn+1 = QnR' + S b. Qn+1 = QnR + S' c. Qn+1 = R' S d. Qn+1 = QnR' + S'	1
2.	While converting a JK flip-flop to D flip-flop, instead of connecting an inverter between its J and K inputs, a buffer has been connected. The resulting circuit will act as a. JK flip-flop only b. T flip-flop c. D flip-flop d. SR flip-flop	1
3.	An SR-f/f is created using only two NOR gates with S and R inputs feeding one NOR gate each. If both S and R inputs are set to one, the outputs will be a. Q and Q' both 1 b. No change in circuit output c. Q and Q' both 0 d. Q and Q' complementary to each other	1
4.	The technique where we multiply each digit by 16^n, where *n* is the "weight" of the digit is a. Hexadecimal to decimal b. Decimal to hexadecimal c. Binary to hexadecimal d. Octal to hexadecimal	1
5.	Which of these methods is not a minimization technique? a. Boolean Algebra b. Karnaugh Maps c. Truth Table d. Quine Mcluskey	1
6.	Identify the law: $(A + B) + C = A + (B + C)$ a. Associate Law b. Distributive Law c. Commutative Law d. Redundance Law	1
7.	Which of these is De Morgans Theorem a. (X+Y)'=X'.Y' and (X.Y)'=X'+Y' *b.* $A + B = B + A$ and $A\,B = B\,A$ c. $A + A\,B = A$ and $A\,(A + B) = A$ d. X+X'=1 and X.X'=0	1
8.	This is an example of POS equation a. (A+B)(A+C)(B+C) b. AB+BC+AC c. (A+B)C+A(B+C)+B(A+C) d. A+AB+ABC	1
9.	K-map numbering follows which number system a. Binary code b. Gray code c. ASCII code d. Octal code	1
10.	Which gates are called universal gates a. AND and NAND b. NAND and NOR c. OR and NOR d. AND and OR	1
11.	For a logic family, given that VOH is the minimum output high level voltage VOL is the maximum output low level voltage VIH is the minimum acceptable input high level voltage	1

VIL is the maximum acceptable input low level voltage
Then correct relationship is

a. VIH > VOH > VIL > VOL
b. VOH > VIH > VIL > VOL
c. VOH > VIH > VOL > VLL
d. VOH < VIH < VIL < VOL

12. A full adder can be realized using
    a. one half adder, two AND gates
    b. two half adders, one OR gate 1
    c. two half adders, one AND gate
    d. two half adders, two AND gates
13. Which of the following is not a property of CMOS logic gates?
    a. High switching speed
    b. Low static power consumption 1
    c. High packing density
    d. High noise margin
14. The race around condition occurs in a J-K flip-flop when
    a. both inputs are 0
    b. both inputs are 1 1
    c. the inputs are complementary
    d. J=0 and K = 1
15. Which of the following statements is false regarding signals and variables in VHDL?
    a. Signals must be declared inside a process.
    b. Signals follow the notion of 'event scheduling' 1
    c. Variables get updated instantaneously without any delay.
    d. VHDL is a hardware description language
16. VHDL and Verilog are
    a. Software description language
    b. Assembly language 1
    c. Hardware description language
    d. Design language
17. The number "00101110" when converted to BCD is
    a. 01000110
    b. 00100110 2
    c. 01010100
    d. 01000111
18. Consider a 4-bit adder with inputs A = {A3 A2 A1 A0} and B = {B3 B2 B1 B0}. For which of the following input condition no carry-out would be generated. (Assume there is no carry input)
    a. A = {1011}, B = {0101}
    b. A = {1011}, B = {0001} 2
    c. A = {1011}, B = {0100}
    d. A = {1001}, B = {0101}
19. simplifiy the given boolean expression ABC + A'B + ABC' to minimum numbers of literals
    a. B
    b. 1 2
    c. A
    d. AC
20. What is the binary equivalent of
    27.1875 decimal
    a. (11011.1101)2
    b. (11011.0011)2 2
    c. (11101.1001)2
    d. (11011.0001)2

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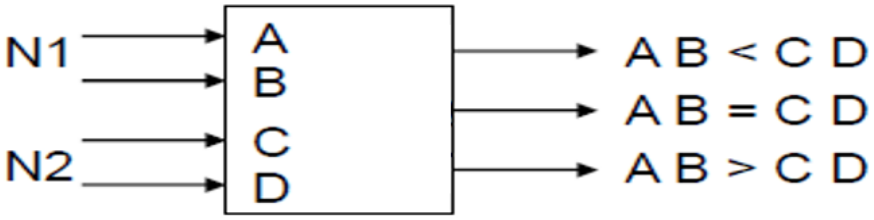
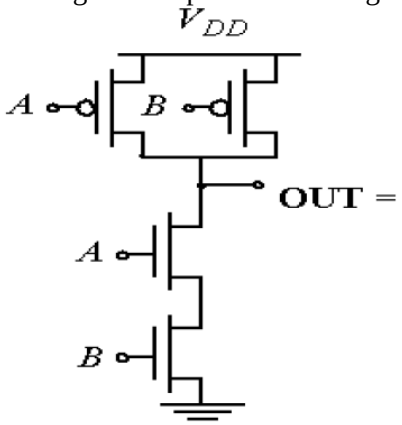
21. This circuit implements



2

a. Two-Bit Comparator
b. Four-Bit Comparator
c. One-Bit Comparator
d. Three-Bit Comparator

22. Which gate is implemented using this circuit at o/p OUT?



2

a. NOR
b. NAND
c. AND
d. OR

23. Implement the function of the following truth table

A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

2

a. X=A'B'C+AB'C+ABC'
b. X=AB'C+AB'C+ABC'
c. X=A'BC+AB'C+ABC'
d. X=A'BC+ABC+ABC'

24. Convert (25) decimal to hexadecimal
a. 31H
b. 19H
c. 25H
d. 33H

2

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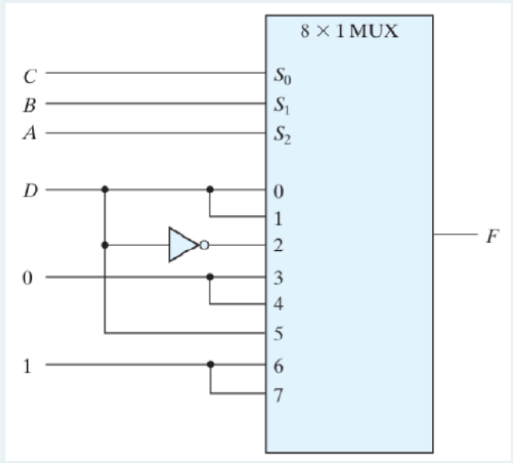
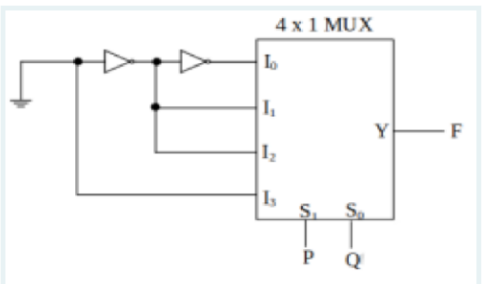
25. Convert 101011_2 to decimal
    a. 43d
    b. 23d 2
    c. 04d
    d. 18d
26. What is $1F0C_{16} = ?_8$
    a. 17414
    b. 14717 2
    c. 17444
    d. 17141
27. Convert 125 decimal to binary
    a. 1111101
    b. 1011101 2
    c. 1111100
    d. 0111101
28. Two's complement of 1011010100 is
    a. 100101100
    b. 100101011 2
    c. 100101101
    d. 100100011
29. The Boolean equation for following function is: $F(x,y,z) = \sum (1, 6, 7)$
    a. $x'y'z + xyz' + xyz$
    b. x'y'z'+x'y'z+xyz 2
    c. x'y'z'+x'y'z+xy'z
    d. xyz+xyz'+x'yz'
30. Identify the output of the following circuit



2

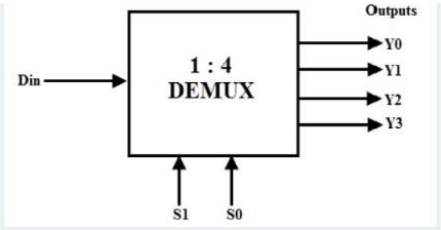
    a. F (A, B, C, D) = Σ(1, 3, 4, 11, 12, 15)
    b. F (A, B, C, D) = Σ(1, 3, 4, 11, 12, 13, 14, 15)
    c. F (A, B, C, D) = Σ(0,2,5,6,7,8,9,10)
    d. F (A, B, C, D) = π(1, 3, 4, 11, 12, 13, 14, 15)
31. Identify the output of the following circuit



2

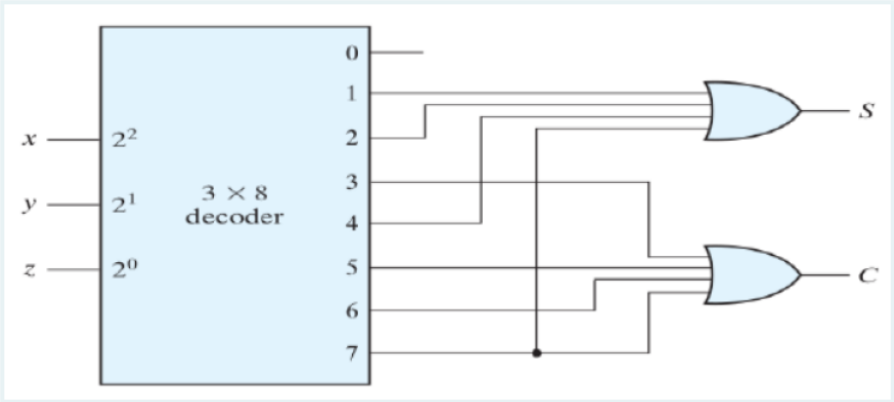
    a. F = P xor Q
    b. F = PQ
    c. F = P+Q
    d. F = P xnor Q

32. Consider the 1:4 demultiplexer circuit shown. What would be the output bits for input condition S0 = 1, S1 = 1 and Din = 1? 2



a. Y0 = 0, Y1 = 1, Y2= 1, Y3 = 1
b. Y0 = 0, Y1 = 0, Y2= 0, Y3 = 1
c. Y0 = 0, Y1 = 0, Y2= 1, Y3 = 0
d. Y0 = 0, Y1 = 0, Y2= 1, Y3 = 1

33. Find the function implemented by the following circuit 2



a. Half adder
b. full subtractor
c. full adder
d. Multiplier